AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1-15 (canceled).

Claim 16 (new): A method for manufacturing a chip electronic component-mounted ceramic substrate, comprising the steps of:

mounting a chip electronic component including a ceramic sintered compact defining an element assembly and terminal electrodes on a ceramic green body having conductors thereon such that the terminal electrodes are brought into contact with the corresponding conductors; and

firing the ceramic green body having the chip electronic component so as to integrate the conductors on the ceramic green body with the corresponding terminal electrodes of the chip electronic component by sintering.

Claim 17 (new): The method for manufacturing a chip electronic component-mounted ceramic substrate according to Claim 16, wherein the ceramic green body is defined by a ceramic green sheet, and a green ceramic stack formed by stacking the ceramic green sheet having the chip electronic component and other ceramic green sheets is fired.

Claim 18 (new): The method for manufacturing a chip electronic component-mounted ceramic substrate according to Claim 17, further comprising the step of:

forming a constraining layer on at least one of an uppermost layer and an internal layer of the green ceramic stack; wherein

the constraining layer primarily includes a sintering-resistant powder that is not substantially sintered at the sintering temperature of the ceramic green sheets.

Claim 19 (new): The method for manufacturing a chip electronic component-mounted ceramic substrate according to Claim 18, wherein the constraining layer is a sheet including the sintering-resistant powder and an organic binder.

Claim 20 (new): The method for manufacturing a chip electronic component-mounted ceramic substrate according to Claim 19, wherein the sheet of the constraining layer is formed on the uppermost layer of the green ceramic stack, and the method further comprises the step of pressure-bonding the constraining layer to press the chip electronic component into the ceramic green sheet.

Claim 21 (new): The method for manufacturing a chip electronic component-mounted ceramic substrate according to Claim 20, wherein the green ceramic stack having the constraining layer is fired with a pressure of about 0.1 MPa to about 10 MPa being applied thereto.

Claim 22 (new): The method for manufacturing a chip electronic component-mounted ceramic substrate according to Claim 18, wherein the constraining layer is formed of a green compact of the sintering-resistant powder on the uppermost surface of the green ceramic stack.

Claim 23 (new): The method for manufacturing a chip electronic component-mounted ceramic substrate according to Claim 16, further comprising the step of:

forming a constraining layer in a sheet form having via conductors arranged corresponding to the terminal electrodes of the chip electronic component, on the ceramic green body to form the conductors; wherein

the constraining layer includes a sintering-resistant powder that is not substantially sintered at the sintering temperature of the ceramic green body and an organic binder.

Claim 24 (new): The method for manufacturing a chip electronic component-mounted ceramic substrate according to Claim 16, wherein the chip electronic component is mounted on the conductors of the ceramic green body with an organic adhesive disposed therebetween.

Claim 25 (new): The method for manufacturing a chip electronic component-mounted ceramic substrate according to Claim 16, wherein the ceramic green body is defined by a ceramic green sheet primarily including a low-temperature co-fired ceramic powder, and the terminal electrodes of the chip electronic component and the conductors on the ceramic green sheet are formed of an electrode material primarily including at least one of silver, copper, and gold.

Claim 26 (new): A chip electronic component-mounted ceramic substrate comprising:

a ceramic substrate having surface electrodes; and

a chip electronic component mounted on the ceramic substrate, the chip electronic component including a ceramic sintered compact defining an element assembly and terminal electrodes; wherein

the surface electrodes of the ceramic substrate are integrated with and sintered to the corresponding terminal electrodes of the chip electronic component.

Claim 27 (new): The chip electronic component-mounted ceramic substrate according to Claim 26, wherein the surface electrodes are bump electrodes.

Claim 28 (new): The chip electronic component-mounted ceramic substrate according to Claim 26, wherein at least a portion of the chip electronic component is embedded in the surface of the ceramic substrate.

Claim 29 (new): The chip electronic component-mounted ceramic substrate according to Claim 26, wherein the ceramic substrate is a multilayer ceramic substrate comprising a plurality of low-temperature co-fired ceramic layers stacked one on top of another, and the terminal electrodes of the chip electronic component and the surface electrodes of the multilayer ceramic substrate primarily include at least one of silver, copper, and gold.

Claim 30 (new): A chip electronic component-mounted ceramic substrate comprising:

a ceramic substrate having surface electrodes; and

a chip electronic component mounted on the ceramic substrate, the chip electronic component including a ceramic sintered compact defining an element assembly and terminal electrodes; wherein

the surface electrodes of the ceramic substrate are connected to the corresponding terminal electrodes of the chip electronic component in a filletless manner without using solder or electroconductive adhesive.

Claim 31 (new): The chip electronic component-mounted ceramic substrate according to Claim 30, wherein the surface electrodes are bump electrodes.

Claim 32 (new): The chip electronic component-mounted ceramic substrate according to Claim 30, wherein at least a portion of the chip electronic component is embedded in the surface of the ceramic substrate.

Claim 33 (new): The chip electronic component-mounted ceramic substrate according to Claims 30, wherein the ceramic substrate is a multilayer ceramic substrate comprising a plurality of low-temperature co-fired ceramic layers stacked one on top of another, and the terminal electrodes of the chip electronic component and the surface electrodes of the multilayer ceramic substrate primarily include at least one of silver, copper, and gold.